

Prior Art
 FIG. 1

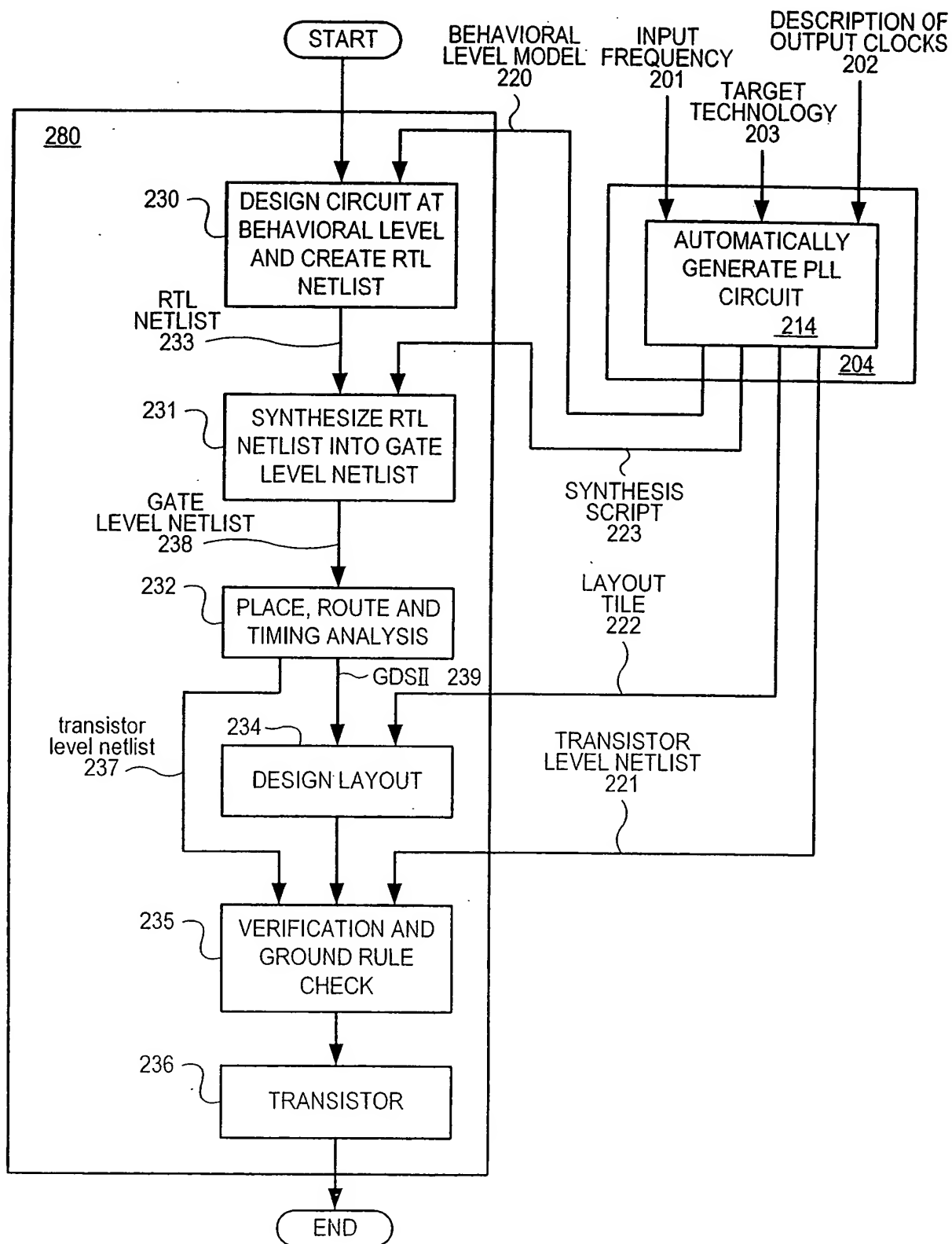


FIG. 2

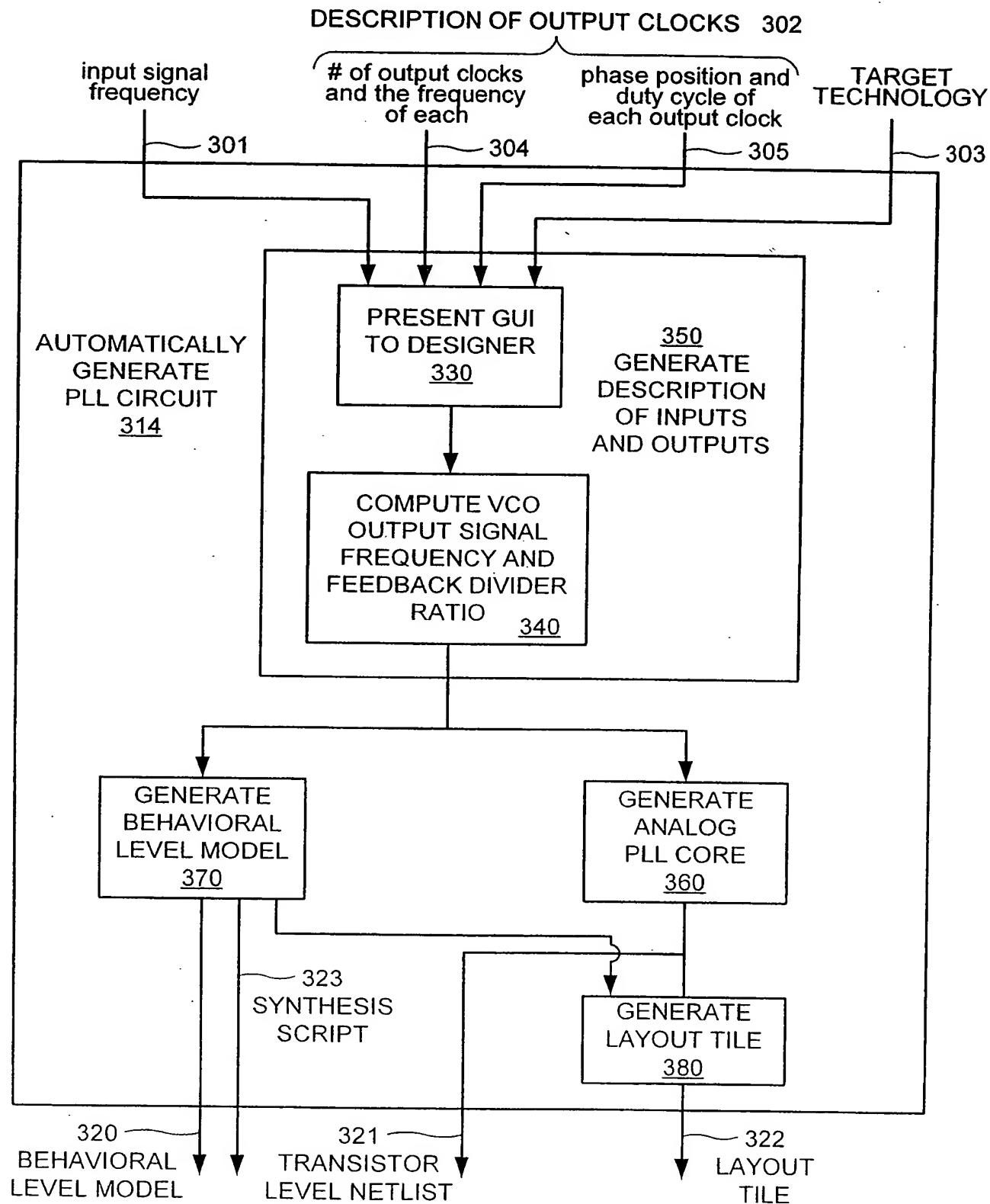


FIG. 3

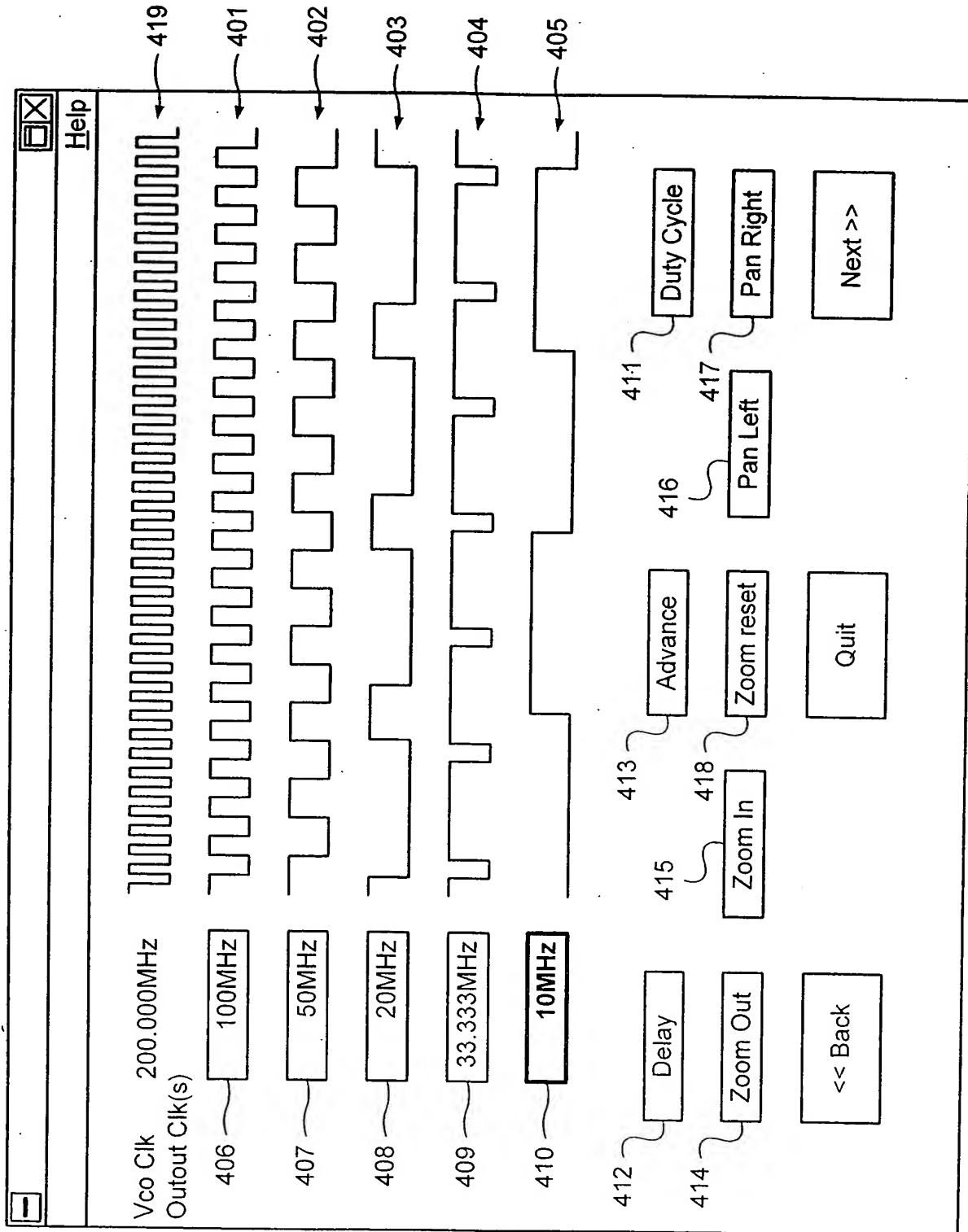


FIG. 4

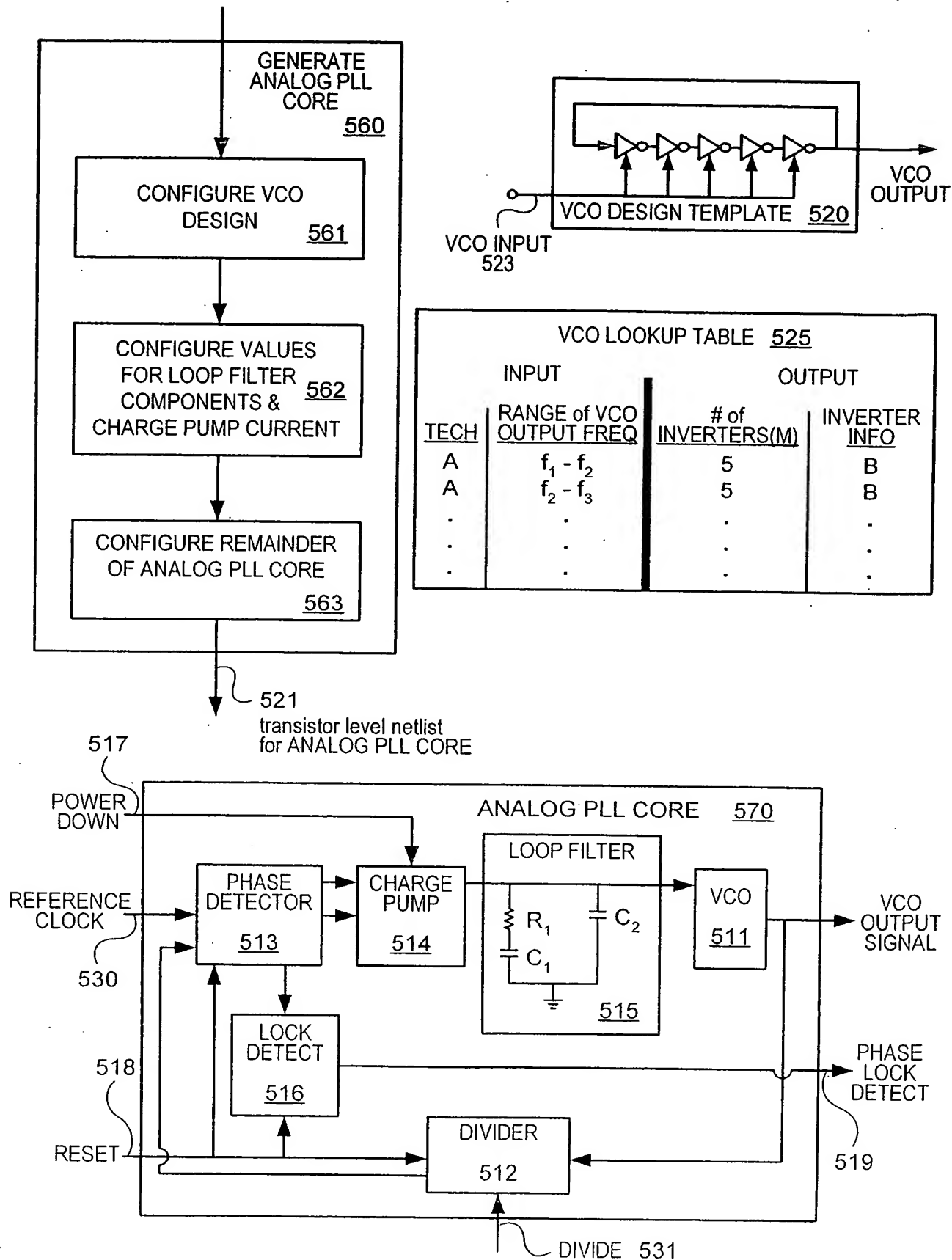


FIG. 5

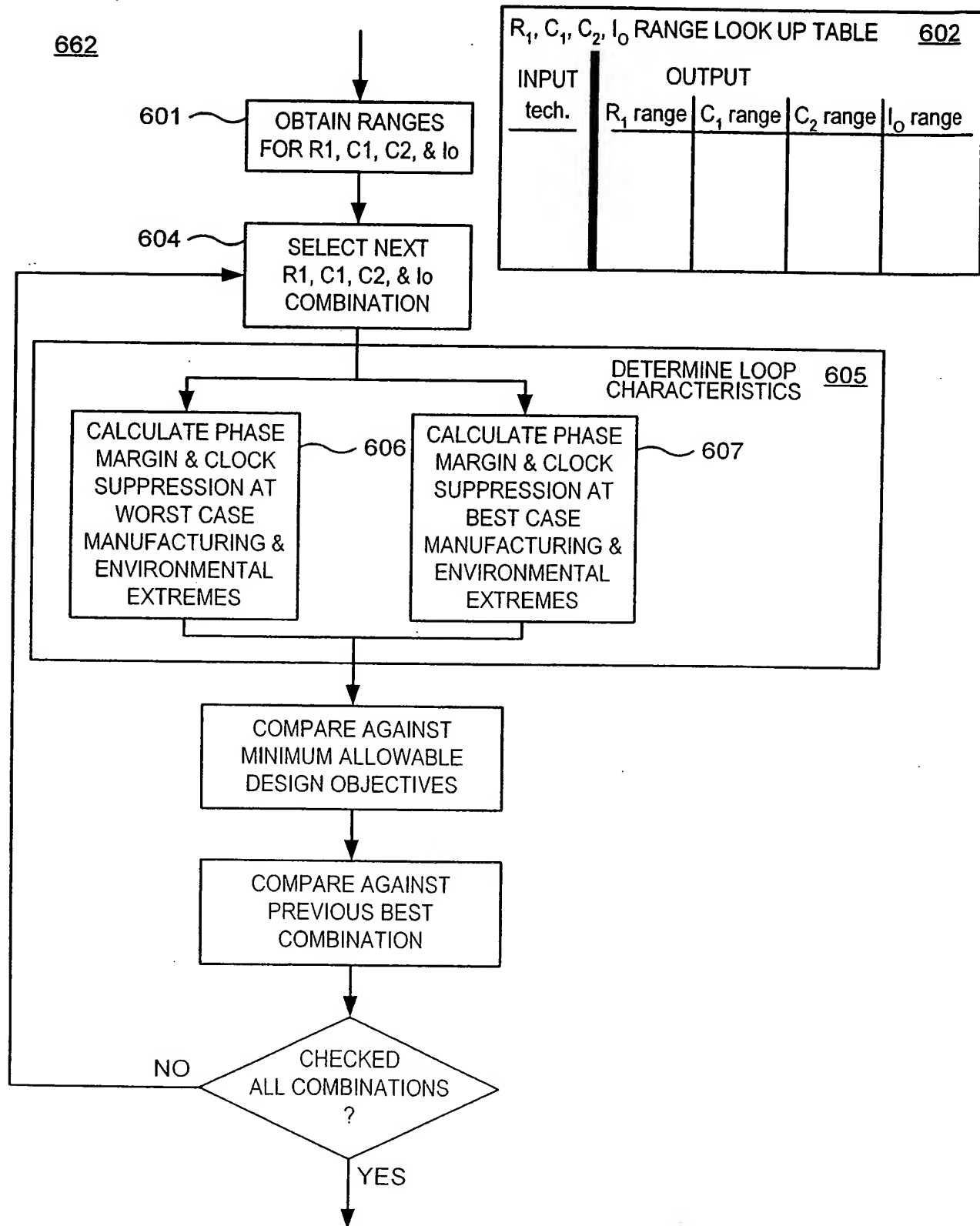


FIG. 6

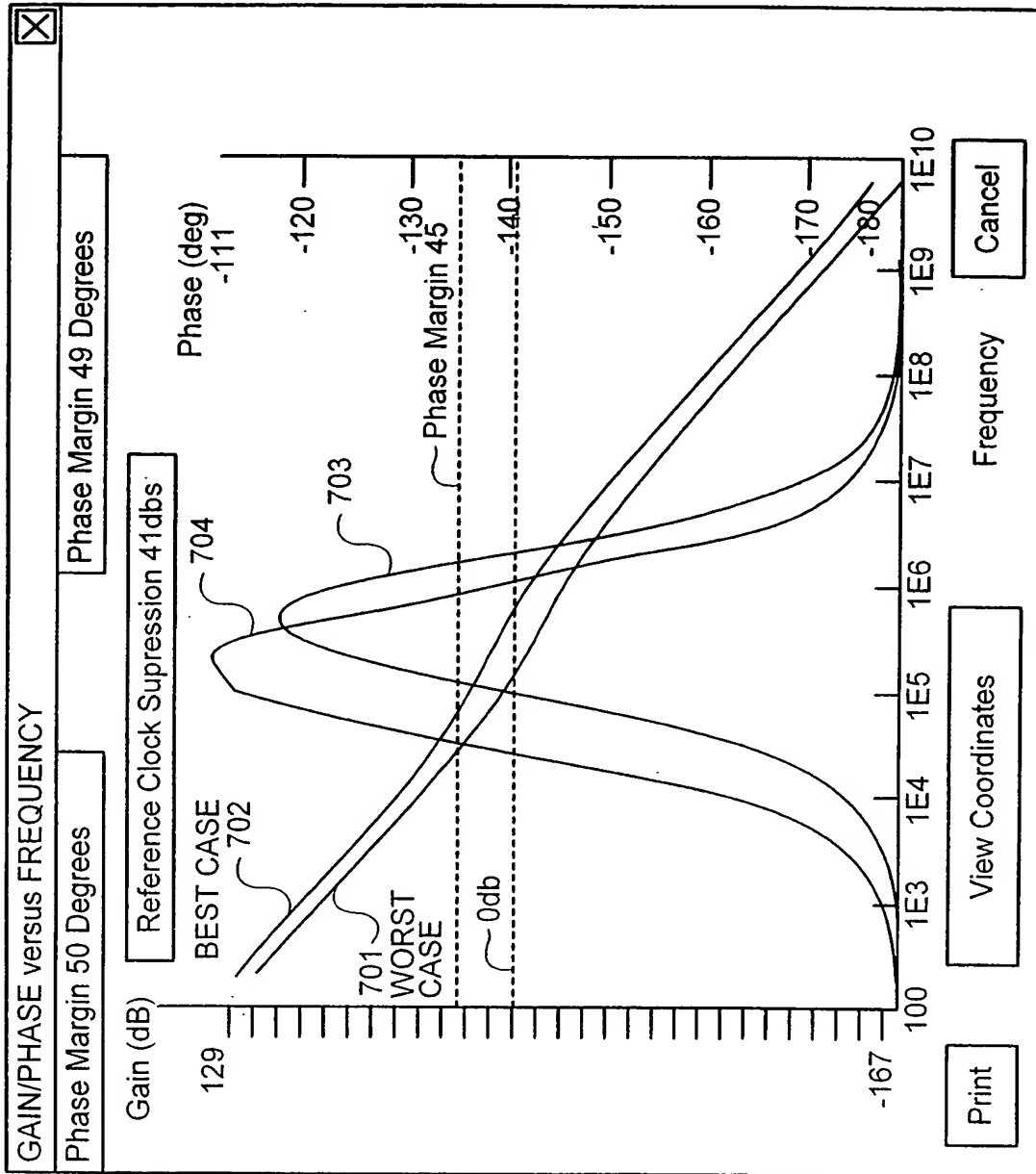


FIG. 7

fast PLL simulator

System Parameters

Kvco [Mhz/V]

116.363636363

R [KOhm]

20

lcp [um]

9

cp[pF]

150

cp[pF]

5

In Freq [MHz]

10

Feedback divider

8

Simulation Parameters

Filter leakage

1e-13

Input Jitter Sigma [pS]

100

Num Cycles

100

☐ Initial Frequency error

☐ Initial Phase Upset

Simulate

Exit

FIG. 8

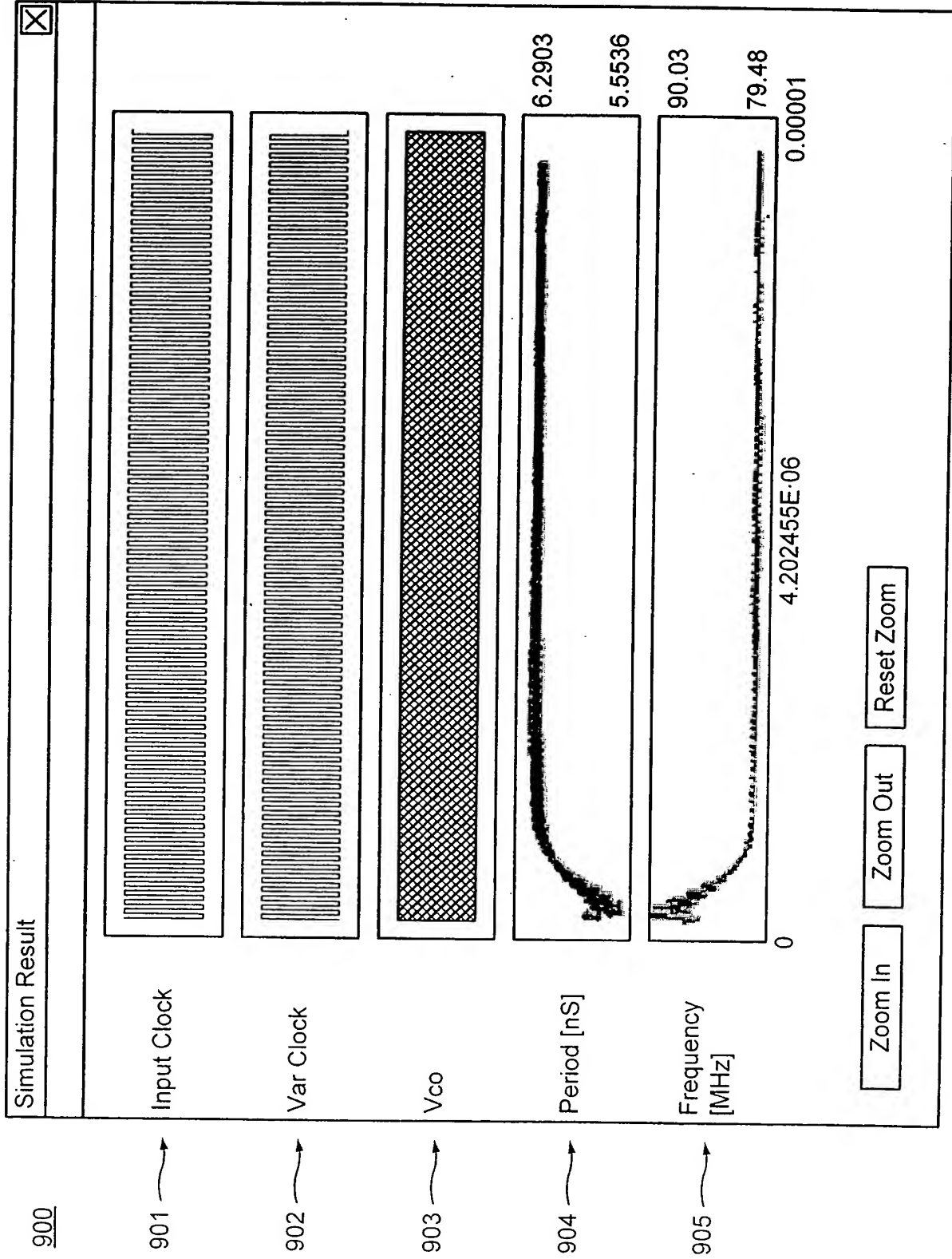


FIG. 9

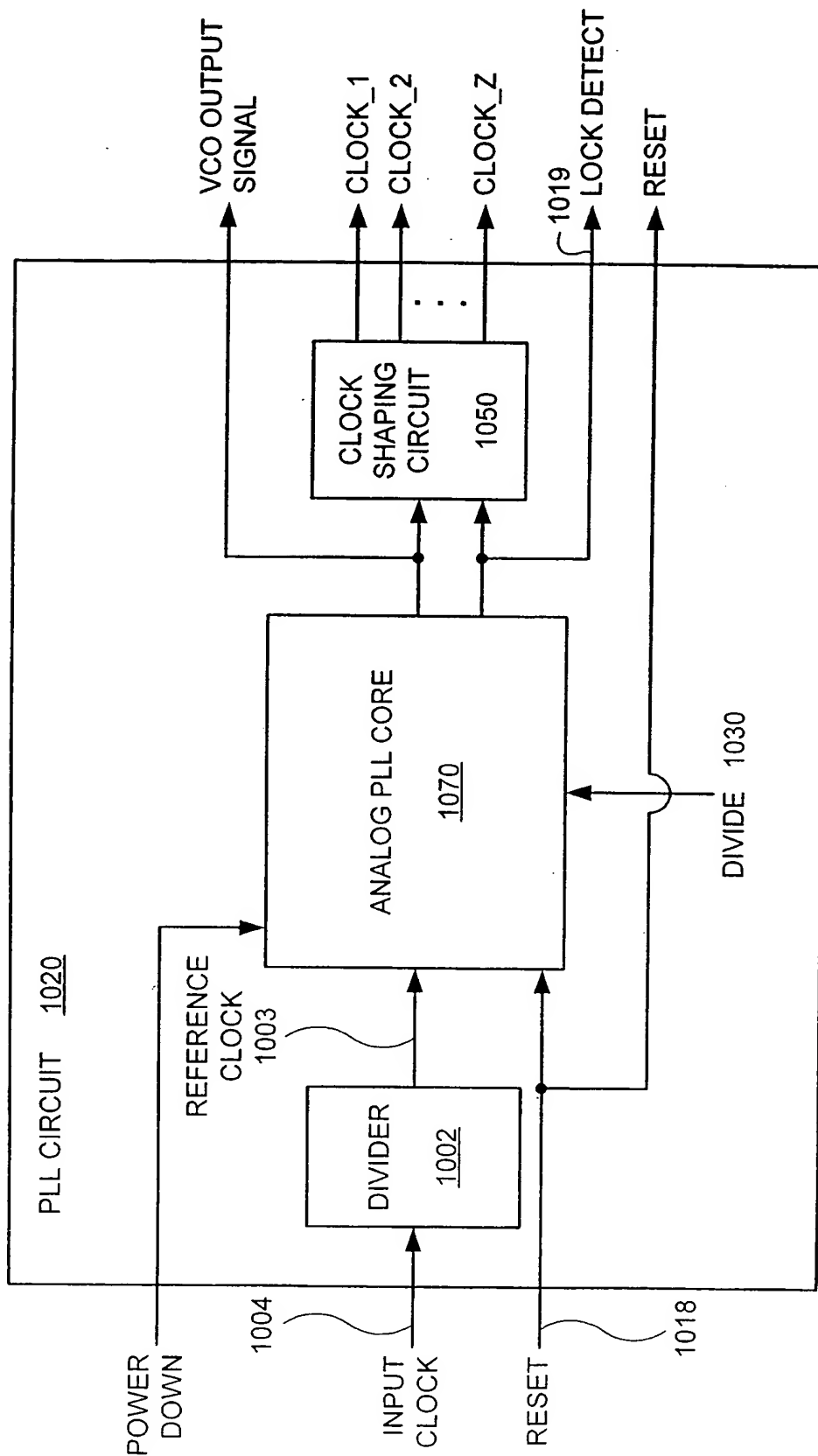


FIG. 10

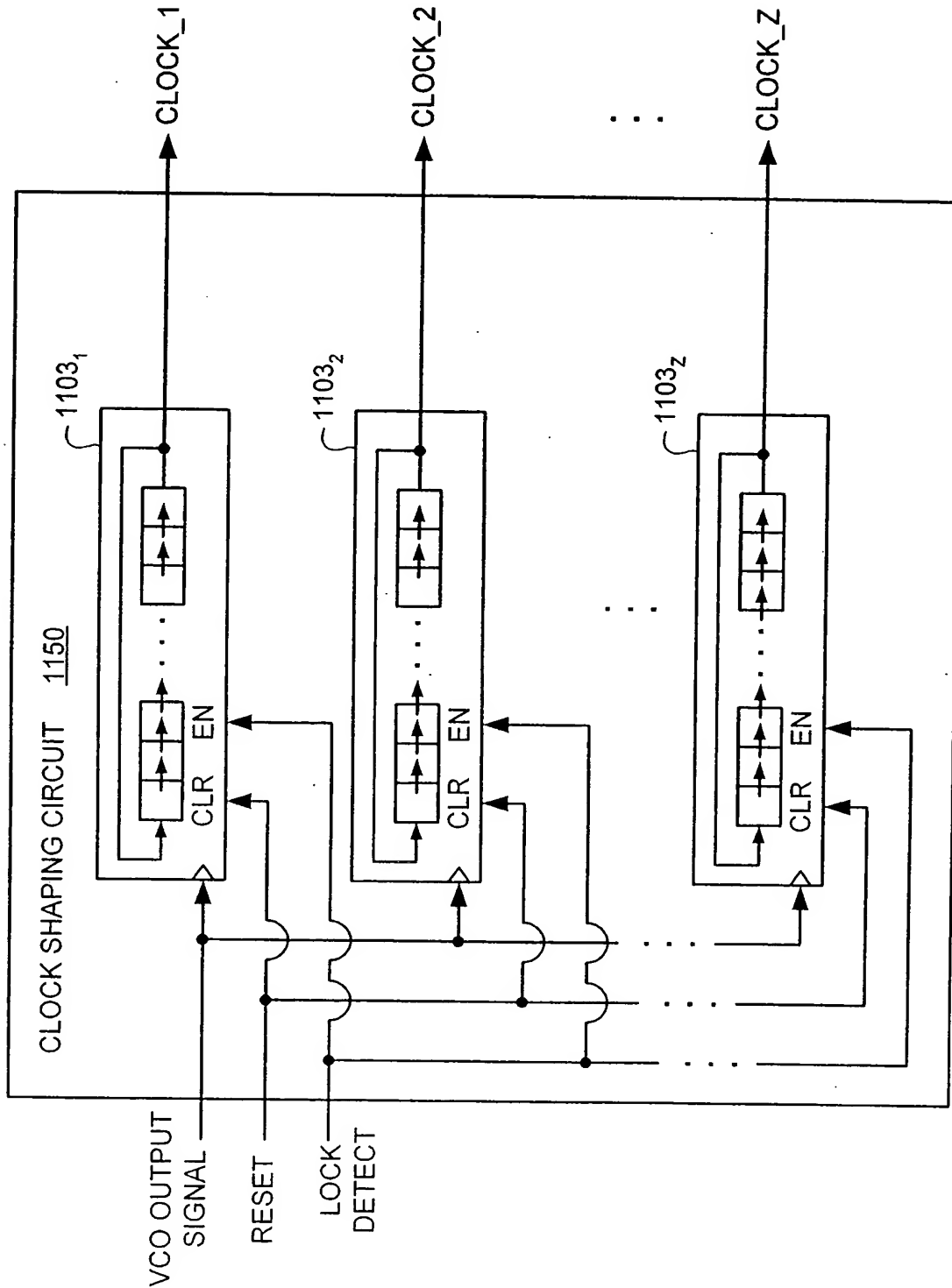


FIG. 11

VCO OUTPUT SIGNAL 1201

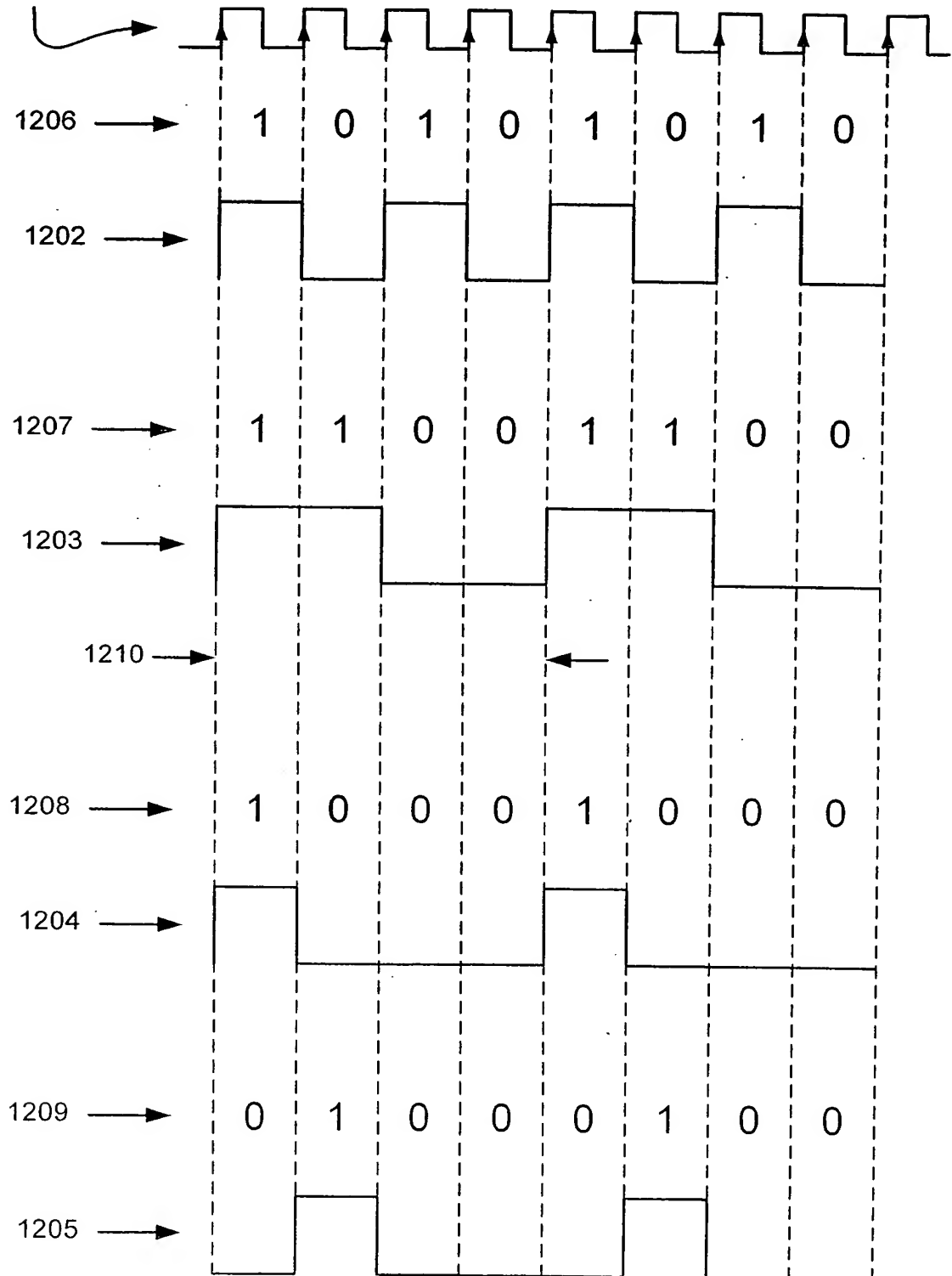


FIG. 12

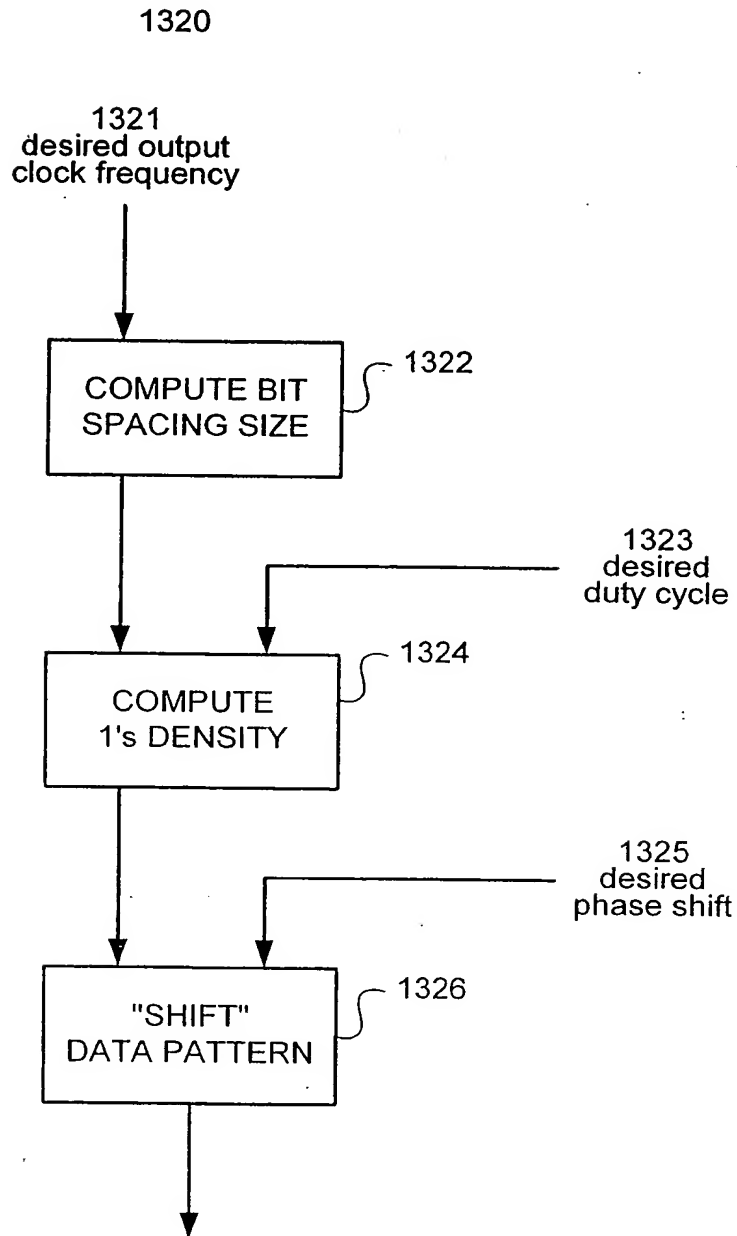


FIG. 13

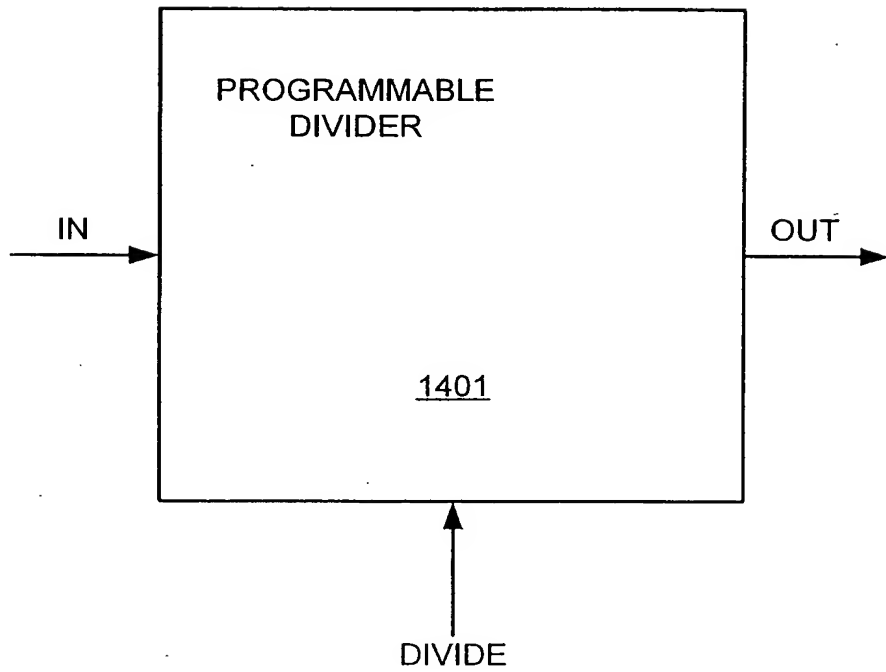


FIG. 14

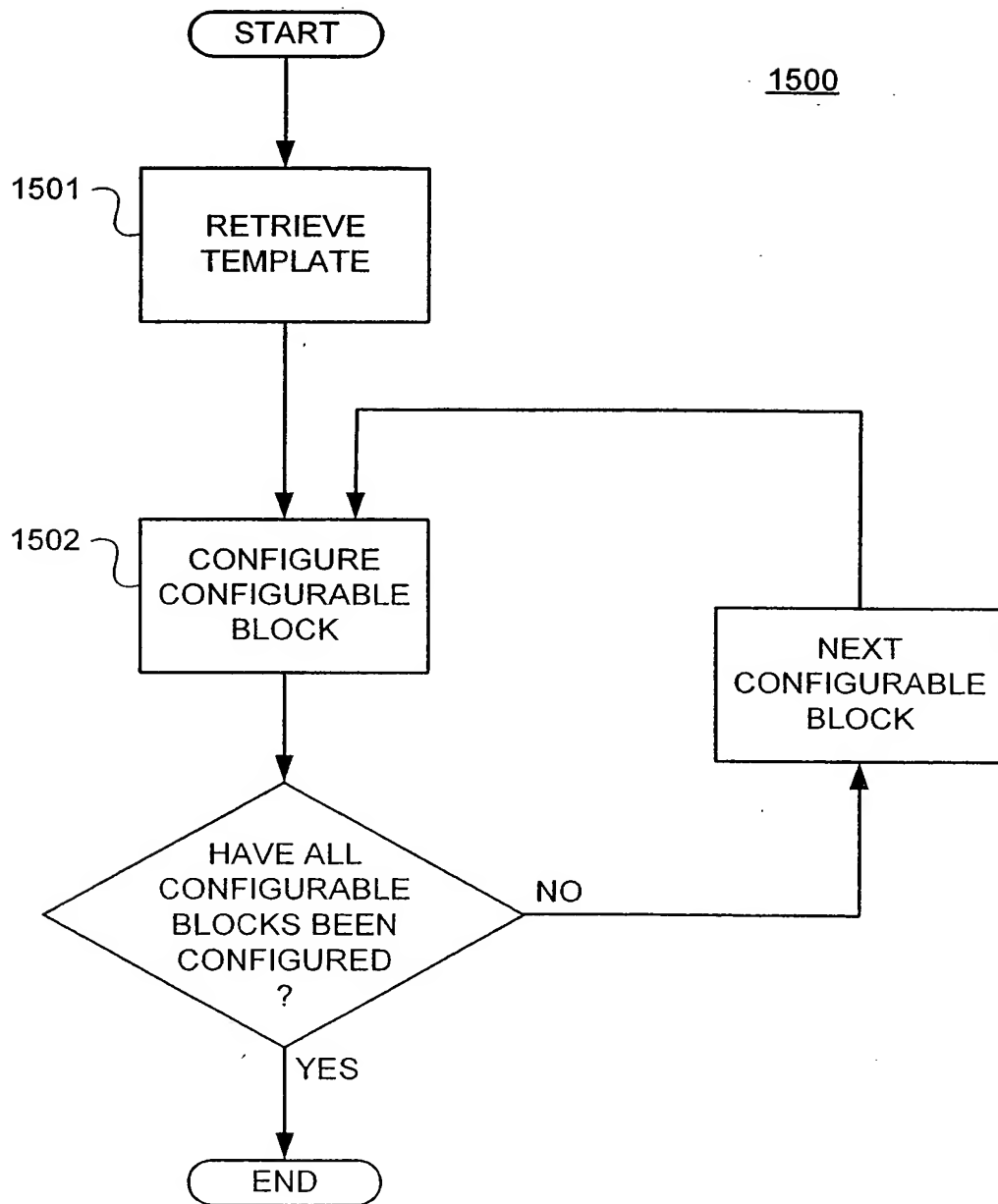


FIG. 15

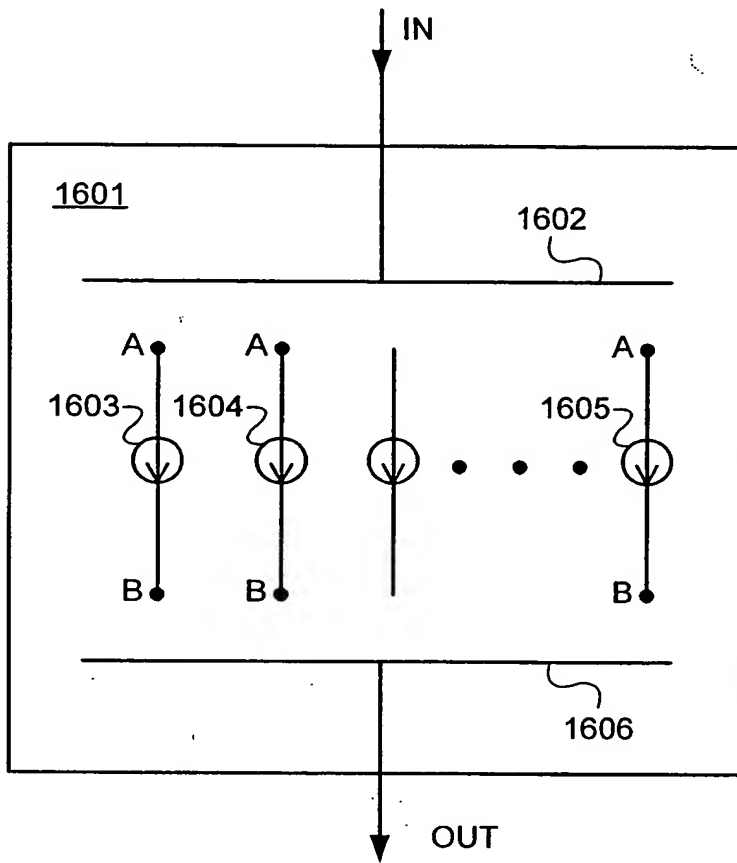


FIG. 16A

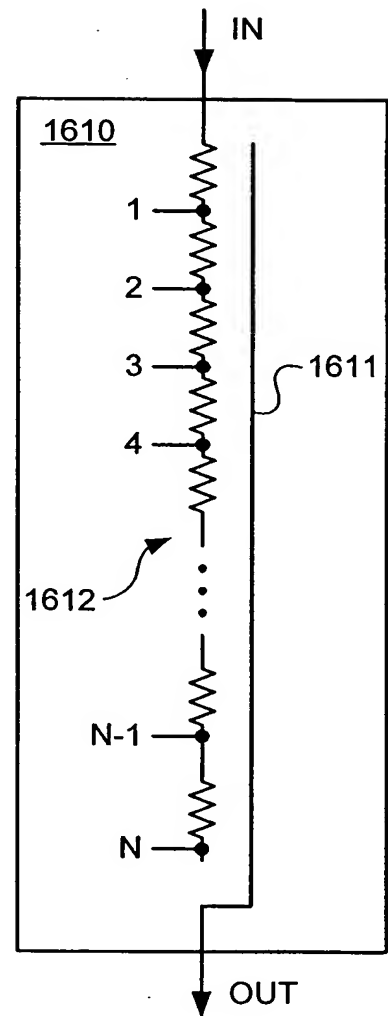


FIG. 16B